REMARKS/ARGUMENTS

The Office Action mailed November 3, 2003 has been received and reviewed. Prior to the present communication, claims 23–33 were pending in the above-referenced application. Each of claims 23–33 stands rejected. Applicants have amended claims 23–26 and 29–31, cancelled claims 27, 28, 32, and 33, and added claims 34–44 herein. Reconsideration of the application is respectfully requested in light of the above amendments and the following remarks.

Specification Amendments

The paragraph beginning at page 6, line 3 and ending at page 6, line 12 has been amended herein to correct a minor grammatical error. It is respectfully submitted that no new matter has been added by way of this amendment.

35 U.S.C. § 103(a) Obviousness Rejections

A) Applicable Authority

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03. In order "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success [in combining the references]. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP §2143 (emphasis added). Further, in establishing a *prima facie* case of obviousness, the initial burden is placed on the Examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been

obvious in light of the teachings of the references. *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)." MPEP §2143. *See also*, MPEP §706.02(j).

B) Obviousness Rejection Based on U.S. Patent 5,472,896 to Chen at al. in view of U.S. Patent 4,782,037 to Tomozawa et al.

Claims 23–33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,472,896 to Chen et al. (hereinafter the "Chen reference") in view of U.S. Patent 4,782,037 to Tomozawa et al (hereinafter the "Tomozawa reference"). As the asserted combination of references fails to teach or suggest all of the limitations of the rejected claims, Applicant respectfully traverses this rejection, as hereinafter set forth.

For the sake of convenience, the independent claims to which the 35 U.S.C. § 103(a) rejection applies are summarized herein. Independent claim 23, as amended herein, recites an *operable* gate stack including a *non-crystalline* metallic silicide film. Independent claim 24, as amended herein, recites an *operable* gate stack including an *amorphous* metallic silicide film, wherein the amorphous metallic silicide film is substantially devoid of silicon clusters. Independent claim 25, as amended herein, recites an *operable* gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting, the operable gate stack comprising a polysilicon layer disposed over the dielectric layer, a *non-crystalline* metallic silicide film disposed over the polysilicon layer, and a dielectric cap on the non-crystalline metallic silicide film. As amended herein, independent claim 26 recites a gate stack structure comprising an *operable* gate stack on a dielectric layer, over a silicon substrate, wherein the dielectric layer is substantially devoid of pitting, the operable gate stack comprising an *amorphous* metallic silicide film which is substantially devoid of silicon clusters. Independent claim 29, as amended herein, recites a semiconductor device comprising at least one *operable* gate stack including a *non-crystalline* metallic silicide film. As amended herein, independent claim 31 recites a semiconductor device, comprising at least one *operable* gate stack structure on a dielectric layer, over a silicon substrate, wherein the dielectric layer is substantially

devoid of pitting, the at least one operable gate stack structure including an *amorphous* metallic silicide film which is substantially devoid of silicon clusters.

By way of contrast, the Chen reference discloses, in a first embodiment, a MOSFET device, and a method for fabricating the same, having a gate oxide layer 12 formed over a semiconductor substrate 10, a polysilicon layer 14 formed over the gate oxide layer 12 and a refractory metal silicide layer 16 formed over the polysilicon layer 14. *See*, *Chen reference*, col. 1, line 57–col. 2, line 5; col. 4, lines 29–36; FIG. 3b. In fabricating the device of the first embodiment, subsequent to formation of the refractory metal silicide layer 16, the structure is etched down to the gate oxide layer 12 as shown in FIG. 3b. Subsequently, a first thin oxide layer 18 is formed over the exposed surfaces of the gate oxide layer 12, the polysilicon layer 14, the refractory metal silicide layer 16, and the semiconductor substrate 10 by thermal oxidation. This thermal treatment transforms the refractory metal silicide layer 16 from its amorphous form into a crystalline form. *See id.* at col. 2, lines 14–20; FIGs. 3c and 4c. Next, a second oxide layer 20 is formed over the first thin oxide layer 18 and the two oxide layers 18, 20 are etched back to form sidewall spacers 20 on the side walls of the gate electrode structure. *See id.* at col. 2, lines 26–34. After formation of the sidewall spacers 20, an ion implantation step is performed to transform the refractory metal silicide layer 16 from its crystalline form back into the amorphous form. *See id.* at col. 4, lines 36–42. Subsequently, a second thin oxide layer 22 is formed over the exposed surfaces of the gate electrode structure and the semiconductor substrate 10 *by thermal oxidation*. *See id.* at col. 2, lines 36–39; col. 4, lines 45–49.

In a second embodiment, the MOSFET device of the Chen reference includes a polysilicon barrier cap layer 30 formed over the refractory metal silicide layer 16, preferably by chemical vapor deposition (CVD). *See id.* at col. 4, line 65–col. 5, line 8; FIG. 4b. Due to the thermal treatment of the CVD process, the refractory metal silicide layer 16 is transformed from the amorphous form into a crystalline form upon deposition of the barrier cap layer 30. *See id.* In fabricating the device of this second embodiment, subsequent to deposition of the barrier cap layer 30 (and thus transformation from the amorphous form into a crystalline form), the barrier cap layer 30, the refractory metal silicide layer 16, and the polysilicon layer 14 are etched down

to the gate oxide layer 12 as shown in FIG. 4b. After formation of the gate electrode structure, ion implantation is performed to transform the refractory metal silicide layer 16 back into the amorphous form. *See id.* at col. 5, lines 9–25. A first thin oxide layer 18 is then formed over the exposed surfaces of the gate electrode structure and the semiconductor substrate 10 by thermal oxidation. Next, using the gate electrode structure as a mask, n-type impurities are implanted into the semiconductor substrate 10 to form n^- lightly doped source/drain regions 13. *See id.* at col. 5, lines 26–37; FIG. 4c. Subsequently, an oxide layer 20 is formed over the first thin oxide layer 18 by CVD . The oxide layer 20 is densified in a nitrogen ambient at a temperature of about 900°C and the oxide layer 20 and the first thin oxide layer 18 are anisotropically etched back to form sidewall spacers 20. *See id.* at col. 5, lines 38–46; FIGs. 4d and 4e. Next, a second thin oxide layer 22 is formed over the exposed surfaces of the gate electrode structure and the semiconductor substrate 10 *by thermal oxidation*. *See id.* at col. 5, lines 47–51; FIG. 4f.

As recognized by both the Specification of the present application and the Chen reference, high temperature steps during fabrication of gate stack structures (*e.g.*, thermal oxidation, CVD, and the like) cause the formation of silicon clusters within the metallic silicide film. *See, Specification* at page 5, lines 19–21; *Chen reference* at col. 2, lines 49–53 and col. 5, lines 5–8. As previously discussed, in the MOSFET device of the first embodiment of the Chen reference, an ion implantation is performed to transform the refractory metal silicide layer 16 from its crystalline form back into an amorphous form. *See, Chen reference* at col. 4, lines 26–42. It is respectfully submitted, however, that in this state, the MOSFET device of the first embodiment of the Chen reference is in an *intermediate* state and is not an *operable* gate stack as recited in each of the independent claims of the present application. Subsequent to the ion implantation in the MOSFET device of the first embodiment of the Chen reference, a second thin oxide layer 22 is formed over the exposed surfaces of the gate electrode structure and the semiconductor substrate 10 *by thermal oxidation*. *See id.* at col. 2, lines 36–39; col. 4, lines 45–49. Thus, while the ion implantation prior to the subsequent thermal oxidation step is stated to reduce the stress in the layer during the thermal oxidation and, accordingly, is stated to positively affect the adhesive properties of the tungsten silicide layer 16, such thermal oxidation will cause

the re-formation of silicon clusters within the tungsten silicide layer 16. *See id.* at col. 2, lines 49–53; col. 4, lines 42–44; *Specification* at page 5, lines 19–21. Accordingly, when the MOSFET device of the first embodiment of the Chen reference is in an *operable* state, it is respectfully submitted that the metallic silicide layer thereof is in a *crystalline* form.

Similarly, with respect to the second embodiment of the MOSFET device of the Chen reference, as previously stated, after formation of the gate electrode structure, ion implantation is performed to transform the refractory tungsten silicide layer 16 back into an amorphous form. *See id.* at col. 5, lines 9–25. It is respectfully submitted, however, that in this state, the MOSFET device of the second embodiment of the Chen reference is in an *intermediate* state and is not an *operable* gate stack as recited in each of the independent claims of the present application. Subsequent to the ion implantation in the MOSFET device of the second embodiment of the Chen reference, a number of high temperature fabrication steps are performed which transform the amorphous refractory tungsten silicide layer 16 back into a crystalline form. In particular, as previously stated, subsequent to the ion implantation step, a first thin oxide layer 18 is formed over the exposed surfaces of the gate electrode structure and the semiconductor substrate 10 *by thermal oxidation*. *See id.* at col. 5, lines 26–37; FIG. 4c. Subsequently, an oxide layer 20 is formed over the first thin oxide layer 18 *by CVD*. *See id.* at col. 5, lines 38–46; FIGs. 4d and 4e. Finally, after an anisotropic etching step, a second thin oxide layer 22 is formed over the exposed surfaces of the gate electrode structure and the semiconductor substrate 10 *by thermal oxidation.* *See id.* at col. 5, lines 47–52; FIG. 4f. It is respectfully submitted that while immediately subsequent the ion implantation step, the metal silicide layer 16 is in an amorphous or non-crystalline form, the subsequent high temperature fabrication steps (*e.g.*, thermal oxidation and CVD) cause the re-formation of silicon clusters within the tungsten silicide layer 16. *See id.* at col. 2, lines 49–53; col. 4, lines 42–44; *Specification* at page 5, lines 19–21. Accordingly, when the MOSFET device of the second embodiment of the Chen reference is in an *operable* state, it is respectfully submitted that the metallic silicide layer thereof is in a *crystalline* form.

Therefore, it is respectfully submitted that the Chen reference fails to teach or suggest an *operable* gate stack including an *amorphous* or *non-crystalline* metallic silicide film as recited in each of the claims of the present application.

It is further submitted that the Tomozawa reference also does not teach or suggest such an operable gate stack structure, nor is it relied upon for such teaching. Rather, the Tomozawa reference discloses a process for fabricating a semiconductor integrated circuit device in which a conductive layer 9(G) is prepared by covering a polycrystalline silicon layer 9A with a layer containing a refractory metal 9B, *i.e.*, a refractory metal layer or a silicide layer of the refractory metal. *See*, *Tomozawa reference* at col. 2, lines 37–47; col. 3, line 54–col. 4, line 15. Over the conductive layer 9(G) is formed an insulating film 11 of silicon dioxide or silicon nitride. *See id.* at col. 4, lines 45–54. An inter-layer insulating film 12 made of phosphosilicate glass (PSG) is formed to cover all surfaces of the conductive layer 9, including the insulating film 11. *See id.* at col. 4, lines 55–61; FIGs. 1B and 7B. The PSG film 12 is then subjected to glass flow at a temperature of about 1000°C. *See id.* at col. 4, lines 65–68.

It is respectfully submitted that at least the high temperature glass flow processing step of the process disclosed by the Tomozawa reference causes the formation of silicon clusters within the refractory metal silicide layer 9B. *See*, *Specification* at page 5, lines 19–21 (high temperature fabrication steps cause the formation of silicon clusters within a metallic silicide film). Further, in some embodiments, the deposition of the insulating film 11 is performed at temperatures high enough to cause silicon cluster formation within layer 9B. *See id.*; *Tomozawa reference* at col. 5, lines 42–48. In any case, the process of the Tomozawa reference does not result in the fabrication of an *operable* gate stack having a *non-crystalline* or *amorphous* metallic silicide film, as recited in each of the claims of the present application.

As neither the Chen reference nor the Tomozawa reference, nor the combination thereof, teaches or suggests an *operable* gate stack including a *non-crystalline* or *amorphous* metallic silicide film, it is respectfully submitted that the asserted combination of references fails to teach or suggest all of the limitations of any of independent claims 23, 24, 25, 26, 29, and 31, as amended herein. Accordingly, it is respectfully submitted that a *prima facie* case of obviousness

cannot be established for these claims based on the asserted combination of references. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As such, Applicant respectfully requests withdrawal of the 35 U.S.C. § 103(a) rejection of these claims based upon the combination of the Chen and Tomozawa references.

Claim 30 depends directly from claim 29 and, accordingly, it is respectfully submitted that a *prima facie* case of obviousness based upon the asserted combination of references cannot be established for this claim for at least the above-cited reasons. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (dependent claims are nonobvious under 35 U.S.C. § 103 if the independent claims from which they depend are nonobvious). As such, Applicant respectfully requests withdrawal of the 35 U.S.C. § 103(a) rejection of claim 30 as well.

Each of claims 27, 28, 32, and 33 has been cancelled by way of the present communication and, thus, the 35 U.S.C. § 103(a) rejection of these claims has been rendered moot.

NEW CLAIMS

Each of dependent claims 34–44 have been added herein. It is respectfully submitted that no new matter has been added and that each claim is supported by the as-filed application.

CONCLUSION

Each of claims 23–26, 29–31, and 34–44 is believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should it be determined that additional issues remain which might be resolved by a telephone conference, the Examiner is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

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